

Infrastructures for Education, Research and Industry in Microelectronics

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Abstract: Infrastructures to provide access to custom integrated hardware manufacturing facilities are important because they allow Students and Researchers to access professional facilities at a reasonable cost, and they allow Companies to access small volume production, otherwise difficult to obtain directly from manufacturers. This paper is reviewing the most recent developments at CMP like the introduction of a CMOS 45nm process, and the cooperation with major infrastructures services available worldwide.

I. THE NEED FOR INFRASTRUCTURES

Infrastructures to provide access to custom integrated hardware manufacturing facilities are important for several reasons:

- they allow Students and Researchers to access professional facilities at a reasonable cost,
- they allow Companies to access small volume production, otherwise difficult to obtain directly from manufacturers.

The needs of Universities, Research Laboratories and Companies can be summarized as follows:

- Universities need to have access to technology for teaching their students. Those students will be in the industry. Therefore they have to be trained at least on the actual state of the art technology processes.
- Research Laboratories usually need to have high performance technologies to validate new concepts. The quality of the research results depends mostly on the quality of the technologies. Accessing to up to date technologies is a necessity.
- Industrial users also need to access to the state of the art of the offered technologies. This is vital for industrial users. The development of a product is usually long (more than 1 or 2 years). It is necessary that an industrial user has access to an up to date process, giving guaranty on product life.

Offering manufacturing Services has to be governed by the following basic principles:

- industrial quality process lines should be used (University process lines cannot offer a stable yield),
- design kits to link CAD and MPC/MPW facilities should be offered to ease the design.

It is also to be noted that almost every country or continent is a high cost country or continent to another one at the time of global markets. It is thus important to keep students, researchers, industrialists ahead of others in order to stay in business. To stay ahead means to train, research, use, advanced design methods and tools and to design on advanced processes.

II. ONE STOP SHOP

A review of early national efforts can be found in [1], and a

review of first cooperative initiatives may be found in [2]. CMP has been developing from a 3.5 NMOS process in 1981 to a 45 nm CMOS process in 2008.

Processes available

Presently the processes available for ICs and MEMS manufacturing are depicted in Table 1.

Austriamicrosystems	0.35 μ CMOS C35B4C3
	0.35 μ CMOS C35B4M3
	0.35 μ CMOS-Opto C35B4O1
	0.35 μ CMOS Flash C35B4E3
	0.35 μ SiGe BiCMOS S35D4M5
	0.35 μ HV-CMOS H35B4D3
STMicroelectronics	45nm CMOS CMOS045
	65nm SOI
	65nm CMOS CMOS065
	90nm CMOS CMOS090
	0.12 μ CMOS HCMOS9GP
	0.12 μ SOI
	0.25 μ SiGe:C BiCMOS7RF
OMMIC	0.2 μ HEMT GaAs ED02AH
	0.2 μ HEMT GaAs ED02AH Bulk Micromachining
MEMSCAP	ASIMPS CMOS + DRIE
	PolyMUMPs
	SOI MUMPs
	Metal MUMPs
CSMC	0.6 μ CMOS 2P/2M/HR
	0.6 μ CMOS 2P/2M/HR Bulk Micromachining

TABLE 1: IC AND MEMS PROCESSES AVAILABLE

ICs design kits and CAD software

Design kits and libraries are distributed by CMP for most of the processes and most commonly used CAD tools. CMP sometimes develop design kits, in cooperation with the manufacturers and the CAD vendors. CMP also offers special CAD software conditions from a few CAD vendors. As a focal point, CMP also distributes information on configuration files, converters, etc. About 40 design kits are available for each process and the main CAD tools.

Other services

Packaging and testing services are also offered. Various types of packages are supported, including DIL, SOIC, CQFP, JLCC, PGA, etc. Test of prototypes is usually done by the final user. On request, especially for low volume production, CMP may take over testing together with manufacturing.

Key figures

Since 1981, CMP has served more than 1000 Institutions from 66 countries in various processes. Support to Industry started in 1993 for small volume production. CMP is ISO 9002-1994 certified from 2000 to 2003. CMP is working on the certification ISO 9002-2000.

Recent developments

Recent developments have been the move to very deep submicron processes: 120 nm CMOS, 90 nm CMOS, 65 nm CMOS and 65 nm SOI, 45nm CMOS, .35 μ HBT SiGe BiCMOS, .25 μ SiGe:C HTB BiCMOS from STMicroelectronics and the exploration of new MEMS fabrication offerings.

The move to very deep submicron processes.

CMP introduced 120 nm CMOS as early as 2001. A total of 175 circuits were fabricated from 2001 to June 2007. CMP introduced 90 nm CMOS in 2004 and nearly 100 circuits have been fabricated up to now. Finally 65nm CMOS was launched in 2006 and a ten of circuits have been fabricated already. This means a total of nearly 300 circuits coming from about 50 Research Laboratories and Industrial Companies. These processes have been very well received. Let’s detail what happened with the CMOS 90 nm. The 90nm CMOS has been announced in 2004, first DRMs and design kits have been shipped to designers in 2004. The list of Institutions who have used the 90nm CMOS to date is depicted in Table 2. One can notice a number of top level Universities in Europe and USA mostly. All Canadian Universities are using the 90nm CMOS process. The move to 65nm has started. The 65nm CMOS has been announced in 2006. The Table 3 depicts the list of Institutions who have received the DRMs and design kits up to now. Again there are many top level Universities in Europe and in USA who are moving to 65nm CMOS.

CANADA : 4	AUSTRALIA : 1
DENMARK : 1	BELGIUM : 2
FINLAND : 2	BRAZIL : 2
FRANCE : 2	CANADA : 13
GERMANY : 1	DENMARK : 2
ITALY : 4	FINLAND : 2
NORWAY : 4	FRANCE : 18
SPAIN : 1	GERMANY : 5
SWEDEN : 1	ITALY : 13
SWITZERLAND : 2	JAPAN : 2
USA : 11	NETHERLANDS : 1
TOTAL: 33 Institutions	NORWAY : 2
from 11 countries	SINGAPORE : 1
	SOUTH AFRICA : 1
	SPAIN : 7
	SWEDEN : 2
	SWITZERLAND : 3
	TUNISIA : 1
	UNITED ARAB EMIRATES: 1
	U.K : 5
	USA : 17
	TOTAL: 101 Institutions from 21 countries
TABLE 2: INSTITUTIONS HAVING SUBMITTED CIRCUITS 90NM CMOS	TABLE 3: INSTITUTIONS HAVING RECEIVED THE 65NM DRMS & DESIGN KITS

Advanced MEMS processes.

For many years, CMP has been offering the MUMPS processes from MEMSCAP: PolyMUMPS, MetalMUMPS, SOIMUMPS. Recently CMP has been moving to SUMMITV from SANDIA and to a MEMS process based on the CMU

post process capabilities.

The SUMMIT (Sandia Ultra-planar Multi-level MEMS Technology) fabrication process is a five-layer polycrystalline silicon surface micromachining process (one ground plane/electrical interconnect layer and four mechanical layers). The MEMS structures made possible by this five-layer planarized surface micromachining process are extremely diversified. CMU post process is a post CMOS processing from Carnegie Mellon University. This post process, applied to an advanced process proposed by CMP (0.35 SiGe BiCMOS from STMicroelectronics), allows to combine on the same chip MEMS structures (resonators, cantilevers, accelerometers, etc.) and microelectronics structures of an advanced BiCMOS process. CMP also introduced a low cost bulk post process micromachining based on a CMOS .6μ from CSMC.

III. PRESENT COOPERATIVE EFFORTS

Presently, the major cooperative effort is undertaken by CMC in Canada, CMP in France and MOSIS in USA. These 3 infrastructure services announced it at DAC in June 2002. Since then, the cooperation has been steadily expanding [3]. CMP has also set up cooperations with ICC in China and with IDEC in Korea.

IV. CONCLUSIONS

A few trends and comments may conclude. The major services are going global in terms of cooperation, acting worldwide. The more advanced services are also going global in terms of technologies, addressing in the future electronics, photonics, mechanics, fluidics, as CMC-CMP-MOSIS plan to do. It is worth to note that the 7 major infrastructure services (CIC in Taiwan, CMC in Canada, CMP in France, ICC in China, IDEC in Korea, MOSIS in USA, VDEC in Japan) share the same legal status: services hosted by a University. The most advanced of these services shared the same development in extending their services from Universities to Companies and evolving from a subsidized service (by Ministries, Agencies, etc.) to a non-profit non subsidized kind of service.

REFERENCES

[1] “MPC Services available worldwide”, invited paper, APCCAS’94 IEEE Asia-Pacific Conference on Circuits and Systems, December 5-8 1994, Grand Hotel, Taipei, Taiwan.

[2] “Infrastructures for Education and Research: from National Initiatives to Worldwide Development”, invited talk, Technical University of Darmstadt, M. GLESNER 60th birthday ceremony, 29 August 2003.

[3] CMC, CMP and MOSIS, “The Scale of Cooperation Increases as the Dimensions of Microchips Decrease”, invited paper, 3rd International Conference on Microelectronic Systems Education, 1-2 June 2003, Anaheim, USA.