

Globalization for Design: A Market for a CMP/IP Repository

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Abstract

Microelectronics, Testbench, innovation:

This paper proposes an "IP Core Marketplace" and Repository for FPGA, ASIC, SoC and other implementations. The sellers would be anyone, most likely independent developers, vendors or universities, selling or promoting their IP goods and services. The consumers would be those firms or entities seeking such goods and services. The "win" for vendors is another channel for selling and market feedback. The "win" for the buyer is an on-demand one-stop shop. This IP Core Marketplace could be further integrated within an IEEE sponsored Global Design Environment to foster the design and implementation of Critical Embedded Systems.

1. Introduction and Motivation

The semiconductor industry is a \$250 billion/year industry [1]. Today any country, firm or entity can and do compete globally in the worldwide marketplace. This is particularly true within the field of microelectronic device design [2], [3]. Once, major firms dominated the industry. They were nearly all located in those few countries that hosted the state-of-the-art microelectronic fabrication facilities ("fabs"), which now cost multi-Billion-US-Dollars to build

"Originally, ICs were designed only by vertically integrated companies with fab facilities. Today, thanks to the past 40 years of electronics design evolution, anyone, anywhere with a PC can become a supplier of sophisticated Microelectronics Systems. They can design with graphical tools, prototype in a Field Programmable Gate Array, transmit the design over the Internet to a remote fab and have the final, tested silicon sent to them by Fedex [4].

Although the semiconductor market is still dominated by the large vertically-integrated semiconductor firms (some 60%) of whom own the necessary fabrication equipment; the primary areas toward which much of the business is being oriented are: selling, marketing and distributing the licensed designs Intellectual Property (IP).

2. Globalization of Design

A number of major developments have made possible the transition from the "Vertically-Integrated" semiconductor company (e.g. Texas Instruments) to the "Virtual Microsystems" company (e.g. Broadcom) including: 1) Mead-Conway's "Design Rules" that allowed the separation of design from fabrication; 2) MOSIS, CMP/Eurochip and the semiconductor fab brokerage; 3) A. Richard Newton's Berkley "Synthesis Project"; 4) Gajski's levels of abstraction from circuits to chips, fostering the design of ASICs; 5) Hardware Design Languages – enabling implementation portability and high-level simulation; 6) FPGA capacity sufficient to implement many designs traditionally done in ASICs; 7) Reusable high-level design components for System on a Chip (SoC) in both ASICs and FPGAs; 8) Globally designed SoCs with reusable virtual components from lower-cost venues

Specifically: Globalization of these Virtual Microsystems companies in general, and the "Globalization of Microelectronic Design," in particular, is primarily due to the "Diaspora of skilled designers." These designers are typically educated in "Western" Universities, obtain their practical experience at "Western" Vertically-Integrated, major Semiconductor Companies; and then they return back to their homelands, or else migrate to wherever the growing design house businesses are located.

3. IP Marketplace Opportunity

In this context, we propose an open, globally accessible "IP Core Marketplace" to support Microelectronic systems implemented with FPGA, ASIC, SoC and other current and future technologies. Our major concern is to insure the availability of reliable cores that form the raw materials for the creation of highly dependable microelectronics that is embedded in our transportation systems and other Critical Infrastructure.

...integrating a multitude of diverse sensors, deployed over global distances, dependent on the reliable operation of a myriad of microelectronic devices....In 2007, recognizing the importance of microelectronics to the global economy's "nervous system," the IEEE Computer Society's Design Automation Technical Committee {tab.computer.org/datc/} created the IEEE Global Education for Microelectronics Systems {I-GEMS}

... to promote and facilitate the global design of microelectronic systems [4].

...Today, the most efficient, and the fastest way to design an SoC is with IP blocks (Intellectual Property block)...[with] standardized interfaces (or “wrappers”).... to layout (VHDL) an SoC [5]

In the IP Market: The Sellers would be anyone, most likely independent developers, vendors, or universities, selling or promoting their IP goods and services. The Buyers would be firms or other entities seeking such goods and services primarily for the purpose of creation of SoC, ASIC, FPGA.

However, there might be Buyers who later might become Sellers -- by integrating several small pieces of IP that they then would Sell to end consumers. For example in the field of communications -- a firm might purchase individual Filter Designs from specialists and integrate them to create the complete IP of the Digital part of a Software Defined Radio (SDR). This SDR would then be made available to an higher level of integrated SoC “builder” who would also incorporate Analog to Digital Converter and RF Amplifiers to “build” the IP for a full Radio [5].

Another firm might then buy the Radio IP and incorporate it with IP for MEMS or even Nano-Sensors to finally actually **Fabricate** a complete chip containing (as an example): 1) Nano-Sensing of Toxic Industrial Chemicals; 2) Signal Processing to continually monitor the concentration; 3) a Full Radio to report an Alarm. This vendor might even offer other SoCs to make up an Overall Monitoring Network providing a form of Ambient Intelligence of the local Environment in a City. This overall Ambient Intelligence Sensing Network [6] could be made up of hundreds of individual Sensing Nodes [7]

The Global Electronics Market has followed the above process using physical devices (e.g. Transistors, Resistors, Capacitors, etc.) that would be “integrated” using Thick or Thin Film wiring into a Hybrid. These Hybrid might then be integrated at the Board Level and then Boards from various suppliers were integrated at the “Box-Level.” We are witnessing the era where all the above can be integrated into a single Complex and Multi-technology System on a Chip [8]

4. Implementation Issues

There are several vendors who offer IP cores with their tools (e.g. MathWorks) or their FPGAs (e.g. Xilinx). There are some board vendors or even box-level vendors who provide their customers with the ability to customize the boards and the incorporated FPGAs (e.g. Lyrtech, Annapolis Microsystems).

There have been some limited examples of a more-open approach to IP distribution mechanism most notably: the Center for High Performance Reconfigurable Computing (<http://www.chrec.org>), the FPGA High Performance Computing Alliance (<http://www.fhpca.org>),

and OpenCores (<http://www.opencores.org>). Finally there was an industry association, the Virtual Sockets Industry Alliance (VSIA) that had established and maintained a series of interface and IP quality standards. However, after 11 years in 2007 it decided to close its operations and transfer the quality IP metric (that had been very commonly downloaded) to the IEEE.

Wakefield, MA, July 9, 2007 —The VSI Alliance (VSIA) [BOD], the leading IP standards body for the electronics industry...has voted to close operations and transfer the work of the VSIA to other organizations who develop IP and electronics standards. The VSIA Board will act as a stewardship committee shepherding the donation of VSIA IP standards....[9]

However, what is primarily missing from all of these is an internationally recognized authority and standards body which would have the means of validating the submitted IP and insuring the users of the quality of the submitted components. The other missing ingredient is a financially viable mechanism for maintaining the necessary infrastructure.

4.1 Role of the IEEE

We propose that the marketplace be a globally accessible **IP Repository** that would be IEEE-sponsored and supported. The IEEE would provide the Repository with the support of a worldwide entity with a Global Reputation for Standards (e.g. IEEE 8.02.11, IEEE 1149, etc.), a membership that adheres to enforceable standards of professional ethical conduct, and intellectual honesty, with the expertise (the world’s largest technical publishing enterprise). This association with the IEEE would encourage further active membership of reputable vendor sources and academic institutions on a global scale.

4.2 I-GEMS and the Repository

In 2007, recognizing the importance of microelectronics to the global economy’s “nervous system,” the IEEE Computer Society’s Design Automation Technical Committee {tab.computer.org/datc/} created the IEEE Global Education for Microelectronics Systems {I-GEMS} Initiative...to promote and facilitate the global design of microelectronic systems.... I-GEMS initial project: is a web-based, globally-accessible Repository for “soft components” to foster collaborative design and implementation...[4]

Ultimately, the **I-GEMS Repository** will store: high quality, reusable trusted “virtual components (IP cores); high-reliability Testbenches for the components, and associated explanatory materials.

Initially, the IP Repository will focus on storing Testbenches that will be peer-reviewed for quality by a peer-review process equivalent to an IEEE Archival Publication. (e.g. “Philadelphia List”) [10].

4.3 IP Marketplace Benefits

The vendors "win" through access to another channel for selling and market feedback. The buyers "win" through the availability of on-demand one-stop shop for IP components. Such an IP Core Repository would provide direct benefits to its members such as:

- Enabling an improved modern academic curriculum [11]
- Enabling academic programs to offer practically educated and ready-for industry students
- Helping to attract or incubate high technology firms within the geographic sphere of participating universities
- A buyers' channel for less expensive, alternative, open or proprietary IP designs tools and support
- A sellers channel to increase sales and market share
- A marketing channel to increase public relations and global exposure
- A resource channel regarding what is available and product reviews

An IP Core Repository could also lead to firms tapping into regions of the world where the math, sciences and engineering skills are strong. This can lead to various competitive advantages for those firms seeking to find out-of-the-box solutions.

Another benefit is that the Repository might enhance the understanding provide a mechanism for enforcement of international copyright laws as they apply to IP cores.

On a social global scale, the IP Repository could provide additional economic "fairness" to various parts of the world, allowing them to effectively compete globally. Local economies could benefit from the Repository, providing beach-heads for global companies to invest, providing new jobs and ancillary businesses such as tourism, finance, etc. The Repository may improve economic relationships between countries and help dispel stereotypes and myths, contributing to better political stabilities.

Those countries, cities, or cultures that place high emphasis on higher education, particularly technology, will be dominant players in this global marketplace. The Repository can lead to establishing more efficient student and faculty exchange among regions (e.g. common IP, projects, and goals). Furthermore, it may assist in building up global recognition for universities, countries, cities or even students themselves (e.g. resume credentials). Finally, a CMP/IP Repository could enable the sharing of expensive (e.g. time consuming IP development) resources saving time and money for faster time-to-market products.

5. Relevant Work at UNH CIDLab

At the University of New Hampshire we have been incorporating the concept of the I-GEMS Repository within our research program and our curriculum in Critical Embedded Systems. Within CIDLab [12] we have been developing some IP components to be some of the first deposits within the Repository [13].

A significant aspect of our work involves developing our GNAT (Global Network Academic Test Initiative) and the "quasi-universal" GNAT gnode (a simple to configure through high level tools such as Simulink from the. MathWorks} quite generic node for a local or global scale network Sensor Node that forms the core of the -- that could be configured / customized -- remotely over the web {e.g. through a site such as Techonline} and be a component of a large / global-scale sensor / actuator network possessing "self awareness and instinctive response [4].

This effort involves:

- Developing the Node itself [14]
- and the tools for those without the knowledge of C programming or FPGA configuration -- who are Subject Matter Experts in a particular sensor, signal processing and /or the overall Critical Embedded Systems Application [15]

5. Conclusion

We propose /IP Repository ("Marketplace") to facilitate the seller and buyer relationship and subsequent purchasing transactions. To be successful the Repository must be reliable and from a trusted source. Our concept of the Repository is supported by the IEEE GEMS Initiative Steering Committee. IEEE will be the sponsor and validating entity for the Repository supplying the market trust enforced through membership, product validations, and consumer reviews.

Our financial model is that of Ebay Corporation and includes: annual membership; insertion fees, which are monthly fees for each IP advertised and; final sale fees (3%-5% fees charged to the seller on completion). Other potential revenue sources would include advertising (pop-up, front page, scrolling), search priority. Initial calculations predict a breakeven point at about 1 year into the business. Subsequently, the aforementioned operating costs, which are estimated to be about \$700K per year, would be met by approximately 100 vendors, each listing 20 items per month and pulling in \$10K per month (or about 60% success rate for the listed IP). Following the practice of MOSIS, we envision a low-cost or free access to university students taking SoC or Embedded Systems Courses.

The Repository can lead to establishing more efficient student and faculty exchange among regions (e.g. common IP, projects and goals). Furthermore, it may assist in building up global recognition for universities, countries, cities or even students themselves (e.g. resume credentials). The Repository could enable the sharing of expensive (e.g. time consuming IP development) resources saving time and money for faster time-to-market products.

Finally, the IP Core Marketplace could be further integrated within an IEEE sponsored Global Design Environment to foster the design and implementation of Critical Embedded Systems [4].

References

- [1] Hoovers (<http://www.hoovers.com>)
- [2] H. Spaanenburg, A. Rucinski, K. Chamberlin, T. Kochanski, and L. Long, "Globally-Collaborative "Homeland" Security System Design", Proc. of the 2007 IEEE International Conference on Microelectronics Systems Education MSE2007, San Diego, CA, June 2007
- [3] D. Bouldin, A. Rucinski and T. Kochanski, "Paradigm Shifts in the Design of Microelectronic System," in: Pursuit of the 21st Century Golden Key, B. Sheu, C.-Y. Wu and M.-D. Ker, Eds, Hsin-Chu, Taiwan: National Chiao Tung University Press, 2007, pp. 4-8 thru 4-187. <http://press.nctu.edu.tw/press-tea/books/2-2.aspx?sn=58>
- [4] T. Kochanski and A. Rucinski, invited paper, "I-GEMS and Global Security," 1st International Conference on Information Technology (IT 2008), May, 2008 at Gdansk University of Technology, Gdansk, Poland
- [5] T. Kochanski, R. Niski, A. Rucinski and J. Zurek, "A Scalable Range Radio-communication Interfacing for Embedded Systems," 1st International Conference on Information Technology (IT 2008), May, 2008 at Gdansk University of Technology, Gdansk, Poland
- [6] K. Lebecki, A. Rucinski, L. Long, and T.P. Kochanski, "Project PLUTO Update: Robots, Wireless Sensors and Synthetic Reality in support of Mine and Tunnel Safety and Security," 2007 IEEE Conference on Technologies for Homeland Security, Boston 2007
- [7] E. Aarts and R. Roovers. "IC Design Challenges for Ambient Intelligence." Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE), Munich, Germany, 3-7 March 2003. IEEE, 2003.
- [8] Dr. h.c. mult. Manfred Glesner, invited talk, "System Design Challenges in the Nano-scale Era," IT'07, Gdansk Poland 2007
- [9] http://www.vsia.org/news/vsia_plans_to_close.htm
- [10] P. Mosterman, D. Boudin and A. Rucinski, "A Peer Reviewed Online Computational Modeling Framework," <http://www.asee.org/conferences/>
- [11] D. Bouldin, T. P. Kochanski, and A. Rucinski, "A Roadmap Towards Microelectronics Education in the Global Era", Proc. of the 2007 IEEE East-West Design & Test Workshop EWD&TW2008, Erevan, Armenia, September 2007.
- [12] A. Rucinski; T.P. Kochanski, B. Rucinska, H. Spaanenburg, and G. Shwaery, "A Laboratory for Critical Infrastructure Protection and Dependability," 2007 IEEE Conference on Technologies for Homeland Security
- [13] B. Rucinska, T. Kochanski, A. Rucinski and H. Spaanenburg, "A Self-Awareness Strategy Using System-Level Diagnosis in CMP/IP-Based Architectures," 2008 IEEE Conference on Technologies for Homeland Security, May 2008.
- [14]] T. M. Jankowski, MS, Technical University of Gdansk "An Architecture and Technology for Ambient Intelligence Node," MSEE Thesis, UNH, 2008
- [15] C. L. Plumlee, BSEE, UNH, "Application Development Process for GNAT, a SOC Networked System," MSEE Thesis, UNH, 2008