

A New Curricula, Oriented at 90nm and Below Technologies

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ABSTRACT

Rapid changes due to integrated circuits (IC) technology nodes shrinking constantly create necessity to develop new curricula which meet the contemporary requirements. It especially refers to 90nm and below technologies in case of applying state-of-the-art low power techniques. This paper describes new developed curricula which fully meets the mentioned requirements and is oriented at using Synopsys EDA tools, created in Synopsys Armenia Educational Department (SAED) and is successfully used in technical universities of Armenia and the region.

1. INTRODUCTION

The evolution of IC development is characterized by technology scaling. It led to the reduction of IC component sizes from several μm to dozens of nm. Technology scaling has significant influence on IC macroparameters:

- Complexity (transistors' count) increases which in its turn leads to the enrichment of IC functional capabilities
- Supply voltage decreases which mainly contributes to the reduction of power consumption
- Performance increases which allows realizing the same transformation of signals in a shorter period of time
- Device density (i.e. the number of transistors per unit area) increases which is aimed at effective usage of silicon area.

It is known that the increase of IC complexity is characterized by Moore's Law [1]. In addition to the fact that within period of time more and more complex ICs are being created, it is also worth emphasizing that the percentage of more complex ICs towards all the ICs being designed also considerably increases [2]. Particularly, statistics show that 30% of designed ICs in 2007 contain more than 8M gates. Increasing complexity and functionality of ICs have resulted producing smaller transistors. Because the electrostatic field strength is proportional to the supply voltage, the latter is also reduced for reliable operation of smaller transistors. For that reason IC power supply voltage constantly drops with the unavoidable scaling of technology. The migration from 0.13 μm to 90nm and below has shrunk supply voltages to 1.2V and below.

Within a period of time the performance of the designed IC also increases. The increase of clock frequency is conditioned by the reduction of parasitic elements and the reduction of differences between signal levels. At present, the clock frequency already reaches dozens of GHz.

The transition into every new technology node naturally leads to the increase of device density, i.e. for the same die size – increase of transistors' number. In particular, at transition from 65nm technology into 45nm that increase makes about 40%.

But the transition into 90 nm and below technologies is not only the reduction of components. In this case first the ratio

of affects on IC operation of different physical phenomena often cardinaly changes. That is, some phenomena which had less affect, became more important, and vice versa. Particularly, if previously gate delay significantly exceeded the one of the wire, then for technologies 90 nm and below, the situation changes dramatically. Another example is the change of ratio of leakage power and dynamic power. If before 130nm technology node the dynamic power considerably exceeded the leakage power (for 0.25 μm technology it was smaller than 5% from power budget) and leakage power could be ignored, then for 90nm technology and below, the situation has sharply changed (for 90nm technology it makes 40-50% and continuing to increase at 65nm and beyond). Other similar examples can also be observed.

On the other hand, for 90 nm and below technologies the effects, which have existed, get worse. In particular, the reduction of IC components sizes results to the increase of parasitic resistances of interconnects and vias. The reduction of power supply voltage, in its turn, leads to the reduction of threshold voltages of separate electronic components, which in its turn reduces the noise margin. Increase of the number of metal layers lead to the increase of cross coupling capacitances, etc. Similar examples are also various.

For 90 nm and below technologies the mentioned change of ratio of physical effects as well as the degradation of the existing effects creates a number of significant new challenges to design 90nm SoCs. They refer to different design aspects – system level design, timing closure, power management, signal integrity, reliability, libraries, tapeout, etc. Each of them, in its turn, contains separate groups of challenges:

- System level design - IP integration, communication centric design, next generation communication paradigm (Networks on Chip)
- Timing closure - Accurate delay calculation, clock issues, On-Chip variation (OCV), Statistical Static Analysis (SSTA), Multi-mode, multi-corner analysis.
- Power management - power dissipation, power density, leakage, power-gating, multiple voltage islands.
- Signal integrity - IR drop, decoupling capacitances, crosstalk, simultaneously switching outputs (SSO).
- Reliability – electromigration, antenna effects, metal slotting effects and stack effects, soft errors, Design for Manufacturing (DFM)/Yield, Design for Test (DFT).

At present, power management is considered the largest challenge and 2/3 of the design projects made by 90nm technology and below are delayed because of power issues. The other challenges are not less important. For example, signal integrity makes 57% of the challenges, timing closure - 50%, etc.

Such rapid changes constantly create necessity to develop new curricula which meet the contemporary requirements. Such a new curriculum has been developed in SAED and is fit to unique educational model realized in SAED.

2. THE ESSENCE OF SAED EDUCATIONAL MODEL

The essence of the educational model in Armenia is the following. It is based on the Industry/University cooperation. The aim is training of highly-qualified specialists who will meet the qualification requirements of semiconductor industry companies. Studies in all educational programs are anticipated: Bachelor, Master, PhD. Studies include the VLSI Design and EDA specializations. Students obtain their basic education (mathematics, physics, etc.) in the first years of the Bachelor program in the University. After acquiring a basic technical education (after the 4th or 5th semester), the best students are selected on competitive grounds to participate in the joint Industry/University educational program. Further education in the Bachelor program as well as Master program and PhD studies is conducted using specially-developed curricula. Curricula is developed taking into consideration the contemporary requirements of leading companies in the semiconductor industry, along with involvement of the area's best professionals and professors and oriented to the use of Synopsys EDA tools. Studies are carried out in specially-equipped classrooms donated by the Company (located in the premises of the Company or University) where every student has the necessary state-of-the-art hardware and an opportunity to use the donated EDA tools. Teaching as well as supervision of course projects, diploma works, Master theses and PhD dissertations are anticipated to be realized jointly by the leading professionals of the Company and experienced professors of the University. Diploma works, Master theses and PhD dissertations are directed to be close to the actual projects accomplished in the Company.

Certainly, University limitations regarding the educational process is considered while developing the curricula. Total numbers of classes per semester, number of weeks per semester, ratio of hours of different types of studies such as lectures, practice classes, and laboratory works have all been taken into account.

However, in case of SAED model, the University did not present very strict limitations to the Company. Also, it was assumed that in addition to compulsory subjects, the Company could also create some extra classes, for example, the study of EDA tools, contemporary programming languages, etc. This also was relevant to organizing studies in Master and PhD programs. The involved students have an opportunity to obtain individual learning which would offer another opportunity to achieve Company/University mutual benefits.

3. THE DEVELOPED CURRICULA

New developed comprehensive and high quality curricula are anticipated for 2 specializations – VLSI Design and EDA. Classes in Bachelor and Master Programs are anticipated for each specialization. Specialized courses in Bachelor Program are anticipated only in 5-8 semesters. And Master Program mainly includes specialized courses.

VLSI Design curricula for Bachelor Program consist of the following courses: VLSI Design Introduction, Introduction to Circuits, Semiconductor Technology and

Devices, IC Design Introduction, Digital Integrated Circuits, Analog Integrated Circuits, Logic Design, Microprocessor Systems, IC Testing, RF Circuits and Systems, IC Fabrication, IC Simulation Theory.

VLSI Design curricula for Master Program consist of the following courses: Design of Special I/Os, PCB Design, RF IC Design, Mixed-Signal IC Design, Design for Test, Digital Signal Processing, VLSI Design and Verification, Crosstalk and Noise, Modeling and Optimization of VLSI Interconnects, Rad-Hard IC Design, Low Power Design, System-on-Chip Architecture Design, Physical Implementation Flow.

EDA curricula for Bachelor Program consist of the following courses: IC Design, Electronic Design Automation, Semiconductor Devices and Technology, Digital Integrated Circuits, Analog Integrated Circuits, Data Structures, Hardware Description Languages, VLSI Design Algorithms, Optimization Methods.

EDA curricula for Master Program consist of the following courses: Electronic Design Automation, Software Verification and Validation, VLSI Schematic Design Algorithms, Databases, VLSI Physical Design Algorithms, VLSI Design, VLSI Verification Algorithms, Modeling and Optimization of VLSI Interconnects, Low Power Design.

All the courses include presentation slides, lecture notes, laboratory works, practical classes, course projects, exams, homework.

The developed curricula have been translated into English, Russian and Chinese and are now adopted at many universities and colleges. Modules are being adopted across the United States and Europe.

4. RESULTS

The developed curricula have been created and are used in SAED and the experience of last years of its application witnesses that the trained specialists have high quality. It is enough to state that more than 60% of the last graduates studying by those curricula are now gainfully employed by Synopsys, Virage, Ponte and other Companies in Armenia meeting the necessary requirements. That is why many other universities expressed desire to use that curricula. Particularly at present it is used in the following universities: the State Engineering University of Armenia, Yerevan State University, American University of Armenia, Russian-Armenian (Slavonic) State University and Moscow Institute of Electronic Technology. The mentioned list continues expanding. Particularly, the Chinese Academy of Science has expressed desire and started to apply the developed curricula.

REFERENCES

- [1] G.E. Moore, "Cramming More Components Onto Integrated Circuits," *Electronics*, volume 38, number 8, 1965.
- [2] IEEE Times Survey, 2005