

Innovation Educational Project at MIET with the participation of the Cadence Design Corporation

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Moscow state Institute of Electronic Technology (Technical University) is a leading institution of higher education in Russia offering integrated training of engineers and researchers in all aspects of microelectronics and nanoelectronics, focused mainly on integrated circuit and sensor development, design and technology; intelligent microsystem physics and technology; surface nanostructure technology.

MIET has many years' experience in educational and research work in design and development of IC components as well as in training highly qualified specialists in this field. While fulfilling this work, MIET applies widely the experience of educational centers of largest foreign companies and famous universities on the basis of agreements concluded between them and MIET. Among strategic partners of MIET there are a big number of RF academic and research institutions, domestic and foreign holdings and companies.

MIET places special emphasis on developing international cooperation with the world's leading companies (Cadence, Microsoft, Synopsys, Mentor Graphics, PTC, Freescale Semiconductor and others) as well as scientific and educational structures, a number of MIET-based educational and research centers being established in cooperation with them.

The major project is being fulfilled jointly with the Cadence corporation, this program focused on training specialists of Master's level is being fulfilled in MIET in the bounds of the Device and System Design Institute (DSDI). At present about 60 students are taking Master's training course in the DSDI at MIET in accordance with purpose-oriented requests from various companies (12 companies and design centers this year). Over the period of

DSDI operation (first Masters graduated in 2004) 85 graduates have obtained Master's diplomas and Cadence certificates. Figure shows the curriculum for Master's degree training in the DSDI.

Future students of the Institute are selected on the competition basis. The Institute provides all the levels of higher professional education. Master's course attendees study Sun-Solaris/Unix operating systems; VERILOG, VERILOG-A and SKILL design languages; special sections of mathematics and device physics as well as a number of specialized courses on mixed-signal IC design.

An essential part of the elite training of specialists at the DSD institute is internship in leading companies of the field which accounts for more than 70% of the total training time. In particular, these are the following companies: Freescale semiconductors, Russian; Uniq IC's, MDPI at RAS, SI Research Institute at RAS, Angstrom joint-stock company, MCST, Mikron, Elvis, Milandr, IDM and others. The DSD Institute cooperates with some of these companies in academic activity as well. Leading specialists of these companies give classes to the DSD Institute students, which results in updating the curriculum in the DSDI in accordance with the current tendencies in microelectronics development and state-of-the-art microcircuit design.

Master's training course in the DSDI provides for background knowledge in the field of physics of semiconductors, circuit engineering, technological routes and processes. The present project is of innovative character and makes it possible to integrate the RF higher education system into the European system of higher education.

Cadence Academy Net (CAN)

12 term 07.02-25.06 11+8 hours per week	Practice: 2 month	Engl. 4-hr seminar, examination	State exam (April)	DSD 17. ADC, DAC 2 hours (1-hr lecture, 1-hr labs) credit	DSD 18. VLSI testing and control. 3 hours (2-hr lecture, 1-hr labs) credit	DSD 19 System-on-a- chip design. 4 hours (2-hr lecture, 2-hr labs) credit	DSD25 System in Package 2 hours (1-hr lecture, 1-hr labs) credit	20 Preparation of Master's thesis. 8 hours. (April, May)		
11 term 01.09-29.01 17.5+7 hours per week	Practice: 3 day a week	Engl. 4-hr seminar, examination	Philoso phy 3-hr lect., examina tion	DSD10 Special chapters of the AIC electrical design. 2-hr lecture examination.	DSD 11 Circuits for Integr. Telecom .Syst. PLL, CDR and Freq synthesis circuits 2.5 hours (1.5 hr lecture, 1-hr labs) examination	DSD 12 Wideband and RF design 1.5 hours lecture, examination	DSD13 Introduction into SHF facilities. 1-hr lecture, credit	DSD 14 Developing of AIC PDK. 3-hours (1-hr lecture, 2-hr labs) credit	DSD 15 An Introduction to Analog Sampled-Data Circuits Design. Part II 3 hours (2-hr lecture, 1-hr labs) Project, examination	DSD 16 VLSI-on-a- programmable- chip design. 4 hours (2-hr lecture, 2-hr labs) credit
10 term 07.02-26.06 17.5 +7 hours per week	Practice: 3 day a week	Engl. 4-hr seminar, credit	Philoso phy 3-hr lect., credit	DSD 6 Introduction to Low freq analog circuit design 4.5 hours (2-hr lecture, 0.5-hr seminar, 2-hr labs) examination	DSD 7 Digital CMOS block design 3 hours (1-hr lecture) VERILOG. 2 hours labs, credit.	DSD 8 Sensors 1 hour lectures, credit	DSD 9 Layout design of CMOS AIC 4 hours (2-hr lecture, 2-hr labs) credit	DSD 15 An Introduction to Analog Sampled-Data Circuits Design. Part I. 1 hour lecture, credit	DSD22 Cadence- Database, programm languages SKILL, 3 hours 1 hr lecture, 2 hr labs credit	DSD 23 Analytical functions and their applications 1 hour lectures credit
9 term 01.09-28.01 15.5+6 hours per week	Practice: 3 day a week	Engl. 4-hr seminar, credit	Philoso phy 2-hr lect., credit	DSD 1 IC components and their models. 2.5 hours (2h lect, 0.5h labs) examination	DSD 2 Introduction into CADENCE. 3.5 hours (1-hr lecture, 2.5-hr labs) credit	DSD 3 VLSI manufacturin g process. 1.5 hours (1.5-hr lecture) credit	DSD 4 Digital CMOS Standard cell design. Fundamentals of VERILOG. 4 hours (2-hr lecture, 2-hr labs). examination	DSD 5 CMOS LSI electrical design features 2.5 hours (0.5- hr lecture, 2-hr seminar) credit	DSD21 Operational system Sun- Solaris/Unix 1 hour labs credit	DSD24- Technical documents 0.5 hour seminar, (home work) credit