

# Mixed TCAD/Electrical simulation learning

Jean-Marc Gallière and Jérôme Boch

Polytech'Montpellier, University of Montpellier, France

## ABSTRACT

In classical microelectronics engineer curriculum, students have to acquire skills in device physics as well as in analog and digital IC design. As a rule, each course is illustrated in a dedicated CAD tools laboratory. Over time, this method leads to a compartmentalizing of the teaching by putting conceptual barrier in the student's mind. This article proposes a laboratory in which students can mix TCAD electrical and SPICE simulation. With this tutorial, the instructor is able to highlight the possible interdependence between these tools but overall to demonstrate students that associated teachings are linked and share the same objectives.

## 1. INTRODUCTION

During a top/down (or bottom/up) IC design, the data flow crosses several software layers. Usually, each of these layers is related to an abstraction level. For example in Fig. 1, an IC description spread out from a behavioral description in Verilog or VHDL to a logical description after the synthesis process. The underneath layer is the electrical level. Here they are no longer logical gates but transistors and interconnections. At the bottom, the layer considers the transistor in his physic aspect; we are in the Technology CAD (TCAD) universe.

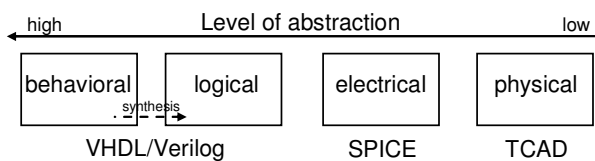


Figure 1: Level of abstraction

In his daily task, the IC design engineer implements simulation tools for each level involved in his area of work. For instance, ModelSim provides a comprehensive simulation and debug environment for complex ASIC and FPGA designs. This tool supports multiple languages including Verilog and VHDL. In this case, behavioral and logical abstraction levels are addressed. At the electrical level, the main simulators are HSPICE, Spectre and Eldo. For the bottom physical layer, two main tools overlook the market of TCAD i.e. Silvaco and Sentaurus (ex. ISE). All this CAD tools hierarchy leads toward a strong compartmentalized teaching and above all prevents students from a global view of the IC design. For that, we propose in this laboratory to show students the link between physical and electrical simulation through the mixed TCAD/electrical simulation ability of Silvaco's software. But above all, the advantage is to place interface teachers between these different levels of abstraction. In this way, contents become intertwined; consequently the student's perception is enhanced.

## 2. TCAD TOOLS

TCAD refers to using computer simulations to develop and optimize semiconductor processing technologies and devices. TCAD simulation tools solve fundamental, physical partial differential equations, such as diffusion and transport equations for discretized geometries. TCAD

consists of two main branches: process simulation and device simulation. In process simulation, processing steps such as etching, deposition, ion implantation, thermal annealing and oxidation are simulated based on physical equations, which govern the respective processing steps. Device simulation can be thought of as virtual measurements of the electrical behavior of a semiconductor device, such as a transistor, or a diode. Again, the device is represented as a meshed finite element structure. Each node of the device has associated properties, such as material type, doping concentration, etc. For each node the carrier concentration, electric field, etc. are computed. Electrodes are represented as areas on which boundary conditions, such as the applied voltage, are imposed.

The main advantage of TCAD tools are visualization, "hands on" experience and marketable skills [1]. Indeed, during process simulation the evolution of actual cross-sections of the structure can be seen. This ability allows a good illustration for the IC processing courses. Moreover, TCAD gives student a chance to learn about realistic silicon wafer processing via hands-on simulation, without the need for IC processing facilities. With TCAD the student can experiment and explore the impact of process flow modifications at virtually no cost. Finally, TCAD simulations are widely used throughout the semiconductor industry.

## 3. LABORATORY

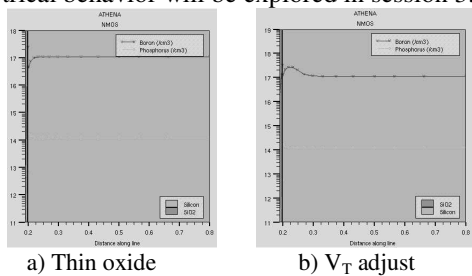
The laboratory occurs in a classroom outfitted with sixteen Sun-Ray clients managed by an UltraSPARC-III sever implemented by the Silvaco suite. The laboratory class is composed of five sessions (4 hours each). All sessions develop two levels of knowledge; the definition/implementation of the simulation script and the analysis/understanding of the results. The Silvaco softwares implemented by the students are ATHENA the process simulator and ATLAS the device simulator. This tutorial occurs early in the student's program. It happens just before a series of tutorial [2] dedicated to the electrical simulation and illustrated by the HSPICE software. Moreover, prior to the beginning of the sessions, a two hours interactive software presentation is conduct by the teacher. This preparatory meeting allows to set up the prerequisites necessary for the continuation of the tutorial namely, doping, diffusion, etc. The component addressed during this introducing laboratory is a diode.

### A. Session 1 - Silicon grounding

The student is introduced to the doping and diffusion processes steps with ATHENA. A P well is created in an initial N doped substrate. By a Boron concentration observation, the student can be aware of the diffusion step importance in the doping process. Student has to tune dose and energy parameters in the implant step and observe the result in the boron concentration profile. The student's objective is to achieve a final  $10e^{17}/cm^3$  Boron concentration in the P well.

For the thin oxide growing, student controls the time and temperature parameters. The oxide thickness is extracted by

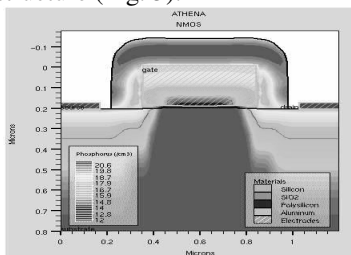
a measurement on the plotted structure (Fig. 2-a). The session ends with a last boron implantation for the transistor threshold ( $V_T$ ) adjust (Fig. 2-b). The concentration effect in the electrical behavior will be explored in session 3.



**Figure 2: Substrate doping and diffusion processes**

### B. Session 2 - Transistor completion

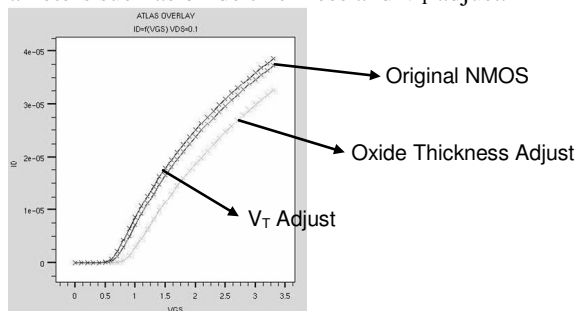
In the first part of the session 2, the polysilicon is deposited and etched at the required gate length size. Because a submicron transistor is addressed in this tutorial, student has to deal with the Lightly Doped Drain (LDD) technological step processes. An initial Phosphorus doping is performed. Afterward, the spacer is deposited and etched on the drain region to allow the last drain Phosphorus doping. The Aluminum contact is deposited and the structure mirrored to obtain the whole NMOS transistor. Finally, the electrode names i.e. gate, drain, source and substrate are added to the structure (Fig. 3).



**Figure 3: NMOS Transistor**

### C. Session 3 - TCAD-Electrical simulation

The student is introduced to the TCAD-Electrical simulator ATLAS. The classical  $I_D=f(V_{GS})V_{DS}$  and  $I_D=f(V_{DS})V_{GS}$  are computed for the previous transistor. In Fig. 4 students have to compute the  $I_D=f(V_{GS})V_{D=0.1}$  electrical characteristics of the obtained NMOS transistor for several process parameters such as oxide thickness and  $V_T$  adjust.

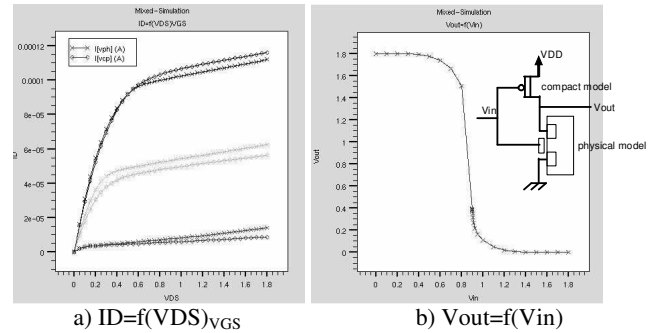


**Figure 4: TCAD-Electrical simulation**

### D. Session 4 - Mixed TCAD-Electrical vs SPICE-Electrical simulation

The mixed device and electrical simulator is introduced. The device electrical  $I_D=f(V_{DS})V_{GS}$  characteristics obtained with TCAD are compared to the same one obtained with a compact SPICE-like model (Fig. 5-a). After, the students have to build a mixed CMOS inverter. This logic gate consists of two different origin transistors: the first one is a NMOS transistor designed with ATHENA and the second

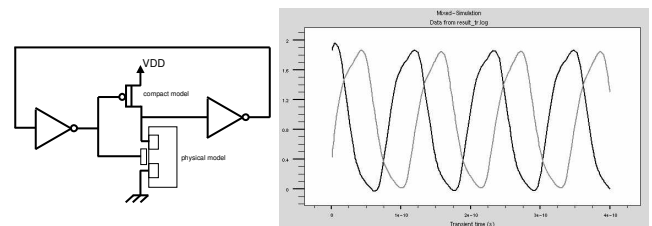
one is a PMOS compact model transistor. Fig. 5-b shows the transfer curve  $V_{out}=f(V_{in})$  obtained by the mixed-mode simulation.



**Figure 5: NMOS Transistor**

### E. Session 5 - Mixed Simulation

In this last session, a ring oscillator with an odd number (3) of inverters is designed by the student (Fig. 6). This structure is classical for monitoring process after IC fabrication. To reduce the computing time, only one transistor springs from ATHENA, the others are compact models. The difficulty of this kind of self-input controlled structure for the simulator is to initiate his computation because potential nodes are not yet setting. For that, students have to use the initial condition simulation directive (.IC).



**Figure 6: Ring oscillator**

## 4. CONCLUSION

For several years, we have observed too much categorizing in microelectronics courses. This partitioning results in teachers working separately from their colleagues. The effect is the students remain with a compartmentalized vision of microelectronics rather than having an overall idea which would be more representative of the reality they will face in their careers. The use of mixed simulation allows students to have a more overall vision of electronics. But the principal consequence is that it has allowed teaching teams from two different worlds (physical and electrical) to meet in order to define together common educational goals.

Furthermore, with this laboratory students develop a wide spectrum of ability in device and electrical simulation. The mixed approach has been used with students for two years. Students are highly satisfied with this approach. Likewise, professors in charge of Analog MOS lectures confirm that the students' perception in electronic systems design has improved.

## REFERENCES

- [1] J. Kenrow, "Integrating Professional TCAD Simulation Tools in Undergraduate Semiconductor Device courses," Proceeding of the 2004 American Society for Engineering Educational Annual Conference
- [2] J.-M. Gallière, "Extensive CMOS and Electrical Simulation Learning," 6<sup>th</sup> International Workshop on Microelectronics Education, 8-9 June 2006, Stockholm, Sweden, pp. 43-46