

Embedded processing support for Digilent FPGA development boards

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ABSTRACT

The Xilinx Embedded Development Kit (EDK) made by Xilinx offers easy-to-build embedded processor systems based on 32-bit soft-core Microblaze or PowerPC processors. However, EDK target boards are usually expensive.

This paper presents the solutions to support Digilent development boards under EDK. Examples of custom cores and solutions for board support files are outlined. The paper also deals with the educational aspects related to teaching embedded processor systems design based on Xilinx EDK.

1. INTRODUCTION

Implementing algorithms on FPGA devices from scratch is done by a state machine implemented using a HDL language. This approach can result in speed and area optimized design. However, as the complexity of the algorithm to be implemented increases, the state machine proves to be an inflexible approach because introducing new states and transitions becomes more and more difficult.

One solution to this issue is offered by the Xilinx PicoBlaze soft-core 8-bit microcontroller [1], which represents in fact a programmable state machine. Though, the microcontroller supports only 1024 instructions and programming can be done in assembly language only.

The Xilinx Embedded Development Kit (EDK) made by Xilinx offers easy-to-build embedded processor systems based on 32-bit soft-core Microblaze or PowerPC processors. These embedded systems made for FPGA-based development boards can be easily used for targeting more complex applications such as complete signal processing solutions or embedded web servers. This is because processor software development relies on GNU C or C++ compiler, and the board peripherals are addressable from the software. Thus, EDK target boards are usually expensive.

A solution for this problem is provided by Digilent. Digilent produces and distributes affordable FPGA-based development boards. Most Digilent boards contain FPGA devices that are large enough to fit a Microblaze soft-core processor, being suitable for embedded processing purposes.

The second chapter illustrates examples of custom peripheral cores designed to support Digilent development boards for embedded processing: A memory controller core that supports both the FLASH and the CDRAM memories on the Nexys and Nexys2 boards and furthermore an On-Chip Peripheral Bus (OBP) compliant EPP controller then a Processor Local Bus (PLB)-compliant EPP controller. The EPP controller can be used to access the Nexys EPP-USB interface from the processor software.

The easiest way to create an embedded processor system under EDK is to use the Base System Builder (BSB) wizard. This wizard automatically inserts the needed peripheral cores, buses and connections into the processor system. This is very useful for students experiencing embedded processor system. In this chapter some particularities in creating the board files for Digilent development boards are also outlined.

In order to teach students how to create their own custom peripheral cores, the Digilent board support cores represent a very good starting example. The next chapter deals with aspects related to teaching embedded processor systems design based on Xilinx EDK. At the end of the paper conclusions regarding the Digilent board support for EDK will be presented and further development directions will be outlined.

2. CUSTOM PERIPHERAL CORES SUPPORTING DIGILENT DEVELOPMENT BOARDS

Although EDK includes many IP cores that are suitable for most of the peripherals used on development boards (such as RAM, FLASH and Ethernet PHY devices), the EDK cores do not cover all of the peripherals or peripheral connections used.

One example is represented by the Digilent Nexys and Nexys2 [2], [3] onboard memory bus that is connected to both a CDRAM and a FLASH memory device. Using the cores supplied by Xilinx EDK, one can build an embedded system containing either the RAM or the FLASH device, but not both. This is due to the fact that Xilinx memory controller cores do not support shared buses.

Therefore a custom memory controller (EMC) core was created that connects to the OPB bus and supports both the Flash and the CDRAM memories.

The EMC supports OPB data bus width of 32 bits. The core allows for 16- and 8-bit accesses using byte enables from the OPB bus. Because the external memory data bus is 16 bit wide, for a 32-bit access the core automatically performs two read or write cycles. Therefore data access size of 8, 16 and 32 bits is possible directly from the software without any extra configuration steps required.

A specific feature of the memory controller is that memory endianness can be changed to support in software memory models of both big and little endian types. In order to achieve this, a Boolean parameter has to be changed from within EDK. The parameter is named `C_USE_BIG_ENDIAN_DATA_FORMAT` and it is linked to the core as a VHDL generic parameter. Note that EDK uses big endianness. The memory controller performs automatically the byte alignment mechanism in order to organize the bytes from the OPB bus according to the

selected endianness. Table 1 shows, for instance, the byte and bit labeling for little endian memory types in the case of a 32-bit wide access.

Table 1. Nexys EMC little endian byte alignment in the case of a 32-bit access

Byte address	n		n+1		n+2		n+3	
Byte Label	0		1		2		3	
Byte Significance	LS byte				MS byte			
OPB Bus bit label	24	31	16	23	8	15	0	7
OPB Bus Bit Significance	MS	LS	MS	LS	MS	LS	MS	LS

Another core example is represented by the Digilent USB-EPP interface. The Digilent onboard USB interface emulates a standard EPP interface. The USB controller on the Digilent boards in conjunction with the Adept software suite provided by Digilent [4] allows data transfer between a PC and a Digilent development board through a PC USB interface.

In order to support the Digilent USB interface under EDK, a custom EPP interface core was made that is compliant with the OPB bus. Due to the fact that data transfer is always initiated from the PC software, the interface uses interrupts in order to signal the microcontroller a data transfer.

A. Digilent board support under EDK 9.2

Starting from EDK version 9.2 the OPB bus has become obsolete and it was replaced by the PLBv4.6 bus. Although the bus interface is changed, for single-beat data transfers the PLB bus is similar to the OPB bus, therefore the EPP core can be easily connected to the PLB bus wrapper component generated by Xilinx EDK Custom Peripheral Wizard, only minor signal name changes are required.

The new version of the memory controller core provided by Xilinx starting from EDK 9.2 allows improved synchronous memory transfer; therefore this core has been chosen for the Digilent board support under EDK 9.2 and above. In order to support both onboard memories that share the address, data and control buses, two separate memory controllers were chosen, one for the CDRAM and one for the FLASH memory. The external signals of the two controllers were connected with a glue-logic multiplexer.

Special care has to be taken for multiplexing the memory data signals, because these signals are bidirectional. EDK generates bidirectional signals for external ports only, using an IOBUFT component. In order to generate an IOBUFT component for a specific signal, there has to be defined a signal group consisting of input, output and three-state enable signals [5]. The data line multiplexing is taking advantage of this property. Therefore this issue was solved by separately multiplexing the data input, output and three-state enable signals.

The board support files for EDK Base System Builder instruct the wizard to insert the memory signal multiplexer without a user intervention. However, the description of the memory controller core provided by Xilinx does not make the data input, output and three-state enable signals accessible from BSB. A solution to this problem was found by slightly changing the original core and make the specific

signals external. In this way the systems built with BSB are correctly accessing the Digilent onboard memories.

3. TEACHING EMBEDDED PROCESSOR SYSTEMS DESIGN WITH XILINX EDK

The BSB wizard is a very good starting point for beginners in EDK, due to the fact that builds a whole hardware system and also offers sample software application only with several simple clicks. In this way students can very easily create their first embedded application.

However, configuring existing peripherals and adding new peripherals require knowledge of the existing processor buses such as the PLB, the Fast Simplex Link (FSL) bus or the Multi-Channel (MCH) bus. This knowledge can be achieved in the easiest way by numerous practical examples. Therefore a good approach to teach embedded processor systems design should be concentrated on laboratory and project work.

The systems build on EDK are taking advantage of the C/C++ language, making very easy the creation of embedded applications for the existing peripherals. Although, taking into account that the processor clock frequency is of 50 MHz on Digilent boards, high-speed applications such as image processing cannot be efficiently implemented in software.

A solution to this issue is to make the signal processing units as cores under EDK and let the software to only control the units. Therefore investment should be made in developing student's skills in custom peripheral creation.

The Digilent board support cores represent a very good starting example, containing a relatively simple code. The designed cores thus bring valuable educational benefits.

4. CONCLUSIONS

This paper illustrates the solutions offered to support the Digilent development boards under EDK. Examples of cores and Base System Builder board support file particularities are outlined. The education benefits of the custom cores and board support solutions are also outlined.

More advanced developments include support cores for the Digilent peripheral modules (PMods) such as SD card interfaces or graphic LCD displays. Further developments for the education of embedded processor systems based on Xilinx EDK include reference designs and components.

REFERENCES

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