

# Building radio systems from digital parts: a HF radio transmitter on a FPGA development board.

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## ABSTRACT

The paper describes a sequence of laboratory exercises focused on designing and building a TX-RX radio chain where all the processing uses digital circuits (SDR approach). The students have access to a high-level codesign environment, which allows to design, simulate and synthesize analog/digital systems. They can explore a variety of design solutions, and use tools very close to industrial practices. The transmitter core is a Direct Digital Synthesizer (DDS), with AM and FM modulation capability. The transmitter uses on-board ADC and DAC, with direct RF output. TX parameters are selectable from the on-board switches. Tx testing is carried out using commercial radio receivers, but also some units of the receiver chain are designed, built, and tested.

## 1. INTRODUCTION

Designing and building a radio systems joins the interest and motivation of students with the chance to explore a variety of functions and technologies. The educational effectiveness can be further enhanced if students can use design tools corresponding to best industrial practices. For these reasons this subject has been selected as leading theme for the sequence of laboratory exercises in the "Telecommunication Electronics II" course held at Politecnico di Torino in 2007.

The goal proposed to students is the design, implementation and test of a complete radio chain (transmitter and receiver) using the SDR (Software Defined Radio [1]) approach that is moving all the processing complexity to the digital domain. The complete task is huge, and must be trimmed and adapted to available time and resource constraints:

- course duration is 7 weeks, with proportional human and material resources assignment.
- the course is focused on hardware design, therefore processing algorithms are translated into VHDL description and FPGA programming.
- the available hardware has limited performances.

This last constraint could be removed by developing a single high-end system on a high-performance FPGA prototyping board (with high-cost). We decided to go in the opposite direction: encourage exploration of different design solutions, by providing the design SW and a development board (Altera DE2, obtained through the University Program [2]) to each student team.

Design specifications are adjusted to take into account these constraints as follows:

- short course duration does not allow the complete development of both the transmitting and receiving parts: we decided to focus the exercises on the TX chain. A first RX chain consist of a commercial radio

receiver (Yaesu FT-847), and some teams designed and built specific units of the receiver.

- the FPGA board can run at 150 MHz clock rate, allowing direct in-band synthesis of acceptable signals up to about 10 MHz (or higher with antialiasing filters).
- The amount of additional hardware is kept to a minimum; ADC and DACs are the units already available in the development board.

To make possible design and testing of several architectures, and to and to provide a view of good practice design process, we used a high-level codesign environment (Codesimulink, [3]). Students learned and used it in a previous course, and therefore were already familiar with the tool.

## 2. STRUCTURE OF THE TRANSMITTER

The block diagram of the transmitter is in figure 1. Going backwards (from "antenna" towards baseband signal), we find the RF output, which uses the on-board video DAC and a short wire antenna. The actual emitted power is very low (also to avoid EMI), and the RF output is not filtered, in order to let student observe on the spectrum analyzer the actual output from a digital synthesizer, and the effect of changes in carrier frequency or sampling rate. Other channels of the video DAC are used to view internal signals (e.g. carrier, modulation, etc.).

The core of the TX chain is a Direct Digital Synthesizer, with direct PM/FM/AM modulation capability. It uses a 16-bit phase accumulator, clocked at the maximum rate allowed by the DE2 board (close to 150 MHz), and a 8-bit sine lookup table. The output frequency could theoretically go up to about 50 MHz (or higher, using the secondary spectra of the sampled signal generated by the DDS). This requires use of good anti alias (analog) filters, and the choice was to use no filter and let students observe the complete generated spectrum (including alias). DDS parameters (frequency, modulation type, modulation index,...) can be set from a on-board control panel, (switches), while LED and a LCD display can be used to observe internal status and variables.

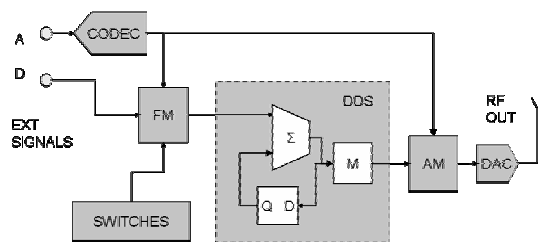


Figure 1: transmitter block diagram

The baseband signal (modulation) is fed to the system through the on-board audio CODEC (A), or through direct digital input lines (D).

### 3. THE DESIGN TOOL

The development is carried out using an high-level co-design environment internally developed at Politecnico di Torino (CodeSimulink). It allows to design, simulate and synthesize VHDL code for any mixed analog/digital system, using an extension of Simulink (The Mathworks). The developed model can be simulated and validated within the MATLAB environment, with the added capability to handle analog units. CodeSimulink dramatically reduces the development phase by direct generation of VHDL or C codes, for implementation on FPGA or DSP, and allows simulation of the whole system in an integrated environment. Cost and performance of different analog/digital or HW/SW tradeoffs, or various architectures for digital units can be easily explored, and various system implementations can be evaluated before going down to the detailed design.

Since the course is focused on digital hardware design, we used the VHDL output for FPGA programming. With DSPs precision is usually not an issue, (floating point variable handled directly by the HW), while FPGA require optimization of resources and power, that means careful evaluation of the number of bits to be used on each step of the processing. The Codesimulink development environment makes possible to modify the variable representation on each unit, and speeds up the design optimization process.

As the design is completed, a compiler translates the building blocks in VHDL using ad hoc developed libraries. Low-level implementation details (like fixed point arithmetic or pipeline levels) are then introduced in a high-level language, and their influence on system performances can be directly evaluated. Synthesis is performed using commercial tools for both ASIC and FPGA like Altera Quartus, Xilinx ISE or Mentor Graphics Leonardo Spectrum, which generate the code to be downloaded on the development board. This approach allows the student to focus only on the high-level algorithm and explore different solutions, with an "automated" implementation, leading to a short development time.

### 4. DESIGN RESULTS

The transmitter uses the DE2 development board from Altera, based on a Cyclone II FPGA, using local DAC and ADC, without external hardware. The high speed triple DAC (SVGA video output), is used for direct synthesis of the RF modulated signal, and the audio CODEC is used for signal acquisition from external sources (MP3 players were used for the lab experiments). Two HF radios were used as test receivers: a Yaesu FT-847 (classic architecture) and a SW radio based on a downconverter which sends digitized IF I/Q components to a PC through a USB interface (CiaoRadio [4]). An example of spectrum of RF signal with AM modulation is in figure 3 (due to the low oversampling rate, the diagram includes the first alias).

Some teams developed also units of the receiver (demodulators). Due to lack of high speed ADC, the "RF" input is the sequence of digital samples generated by the transmitter. Half-wave and full-wave envelope decoder, and a PLL-based synchronous receiver are used for AM and FM demodulation. The PLL is fully digital and exploits the FPGA embedded high-speed multipliers, thus achieving an operating speed of 150 MHz. The channel transfer function can be evaluated by comparing input modulation and demodulated output signal (rebuilt by the audio codec).

### 5. ACKNOWLEDGMENT

The boards used by students in the lab were donated through the Altera University Program.

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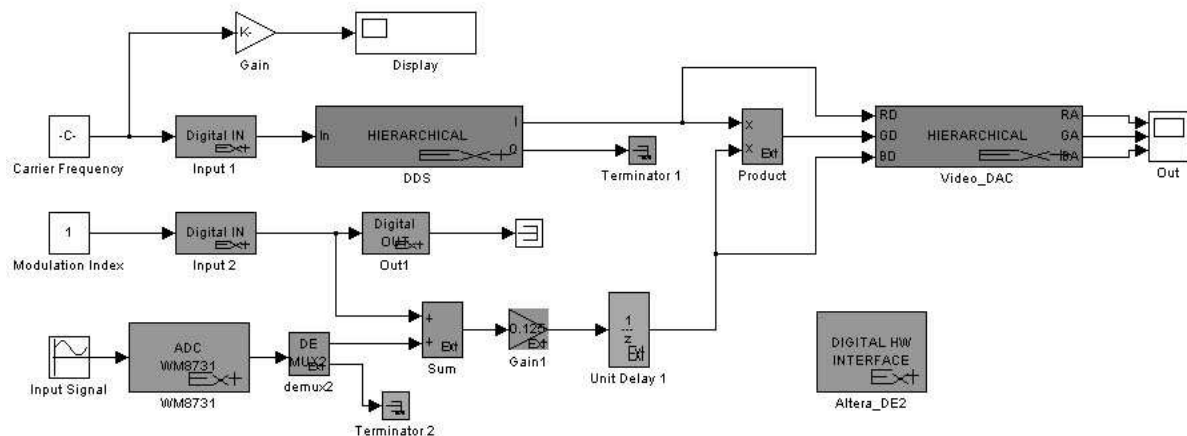


Figure 2: transmitter CodeSimulink block